REMARKS/ARGUMENTS

Claims 1-20 are pending. Claims 1, 7, 12, and 15 have been amended.

Claims 7, 9, 10 are rejected under 35 U.S.C. §103(a) as being unpatentable over Waugh (4,802,441) taken with Kobayashi et al. (6,200,432). Claims 1,2,4-5,7,9-10,12, and 14 were rejected under 35 U.S.C. §103(a) as being unpatentable over Kitamura (6,435,869) taken with Kobayashi et al. (6,200,432). Claims 6,11,15-16, and 18-20 were rejected under 35 U.S.C. §103(a) as being unpatentable over Kitamura (6,435,869) and Kobayashi et al. (6,200,432) as applied to claims 1,2,4-5, 7, 9-10, 12, 14 above and further of Suzuki (2004/0009644). Applicant respectfully requests withdrawal of the rejections in light of the amendment and the following remarks.

In the embodiment of pending independent claim 7, as amended, a method for annealing a semiconductor substrate in a chamber of a single wafer processing furnace is disclosed. The single wafer processing furnace is supported by the specification and Figure 7 shown below.

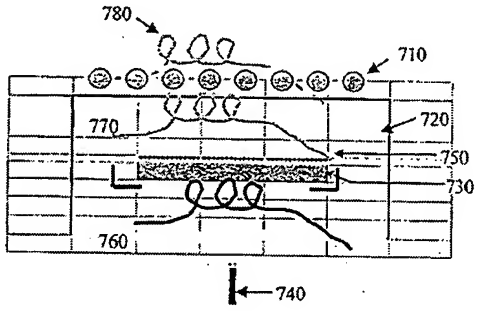


FIG. 7

The method includes heating the semiconductor substrate in the chamber. The method also includes cooling the semiconductor in the chamber. To cool the semiconductor substrate, the method includes flowing a first gas in a vicinity of at least one wall of the chamber, flowing a second gas in the vicinity of at least one heat source and flowing a third gas in a vicinity of the semiconductor substrate.

In contrast, Waugh et al. 1 indicated a fast cool-down furnace. The fast cool-down furnace indicated by Waugh et al. is for "batch processing" of semiconductor wafers and not a single furnace as recited in claim 7, as amended. In addition, the furnace indicated by Waugh et al. includes a double wall cylinder (59 in Figure 1) to provide a gas flow outside the reaction vessel (Column 4, Lines 23-34). The fast cool-down furnace even includes a cage surrounding a batch of wafers and conduits for a gas flow into the cage to promote cooling and positive pressure in the reaction vessel. Other variations include multiple fans outside the reaction vessel to control cooling in different zones within the reaction vessel. Also described in Column 6, Line 67, "to quickly cool down the wafers, the core 92 is slideably removed ... to a position remote from the reaction vessel ...". Accordingly, the furnace indicated by Waugh et al. does not teach or suggest heating a semiconductor in a chamber and cooling of the semiconductor substrate in the chamber in the manner claimed, as recited in claim 7, as amended. The Examiner also cited Kobayashi et al. to allegedly indicate a cooling gas at a temperature lower than room temperature. However, Kobayashi et al. merely relates to a cooling stage for wafers after sputtering and before returning the wafer to atmospheric pressure. Accordingly, Kobayashi et al. does not cure the aforementioned deficiency of Waugh et al. Accordingly, claim 7 is patentable over Waugh et al. even taken with Kobayashi et al. under 35 U.S.C. §103(a). Claims 8-11, and additional features cited therein, which dependent from claim 7, should also be allowed for a similar rationale and others.

Claims 1, 2, 4-5, 7, 9-10, and 14 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Kitamura (6,435,869) taken with Kobayashi et al. (6,200,432). These claim rejections are improper as described as follows.

In the embodiment of pending independent claim 1, as amended, a method for annealing a semiconductor substrate in a chamber of a single wafer processing furnace is disclosed. The method includes heating the semiconductor substrate in the chamber. The method also includes cooling the semiconductor in the chamber. To cool the semiconductor substrate, the method includes flowing a first gas in a vicinity of at least one wall of the chamber,

flowing a second gas in the vicinity of at least one heat source and flowing a third gas in a vicinity of the semiconductor substrate.

In contrast, Kitamura merely indicates a quartz window reinforced with ribs capable of maintaining a negative pressure for a processing chamber. The quartz window includes ribs to allow gas passage to cool the quartz window seal (136 in Figure 8, column 8 lines 49-65) and heating lamp. To cool a wafer after a thermal process, a cooling plate (114A in Figure 21 and Figure 22) can be brought closer to the substrate and a cooling gas is supplied to a space between the cooling plate and the substrate. Accordingly, Kitamura does not teach or suggest the present method of annealing a semiconductor substrate in a chamber of a single furnace in the manner claimed, as recited in claim 1, as amended. As noted, Kobayashi et al. is irrelevant. Accordingly, claims 1 is patentable over the cited references. Claims 2, 4-5 and additional features therein, which dependent from claim 1 should also be allowed at least for these reasons and others.

Applicant submits that claim 7 should also be patentable over the cited references Kitamura taken with Kobayashi et al. That is, claim 7 recites combination of element such as " cooling the semiconductor substrate in the chamber", "the cooling the semiconductor substrate includes flowing a first gas in a vicinity of at least one wall of the chamber, flowing a second gas in a vicinity of the at least one heat source, and flowing a third gas in a vicinity of the semiconductor substrate". Such elements are not taught or suggested by the cited references, alone or taken in combination. Accordingly, claim 7 is patentable over the cited references. Claims 8-11 which dependent from claim 7 should also be allowed at least for a similar rationale and others.

Applicant submits that claims 6,11,15-16, and 18-20 are not properly rejected under 35 U.S.C. §103(a) as being unpatentable over Kitamura (6,435,869) and Kobayashi et al. (6,200,432) as applied to claims 1,2,4-5, 7, 9-10, 12, 14 above and further of Suzuki (2004/0009644).

Claim 6 depends from independent claim 1, claim 11 depends from independent claim 7, and claims 18-20 depends from independent claim 15. As noted above, Kitamura and

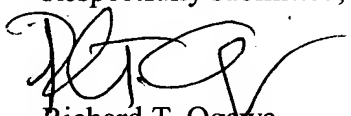
Kobayashi fail to provide any teaching of the method of annealing a semiconductor wafer in a single wafer processing furnace in the manner claimed as recited in claims 1, 7, 12, and 15. Suzuki merely indicates a method of forming source/drain regions and corresponding LDD regions using laser anneal. Accordingly, independent claims 1, 7, 12, and 15, as amended should be patentable over the cited references. Corresponding dependent claims 2-6, 8-11, 13-14, and 16-20 and additional features therein, should also be allowed for a similar rationale and others. Accordingly, all claims should be allowed at least for these reasons and others.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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